

the semiconductor substrate comprises a p-type silicon substrate;  
the source comprises an n+-type source region in the substrate;  
the drain comprises an n+-type drain region in the substrate; and  
the channel comprises a channel region in the substrate between the source region and the drain region.

42.(New) The integrated circuit field effect transistor of claim 2 wherein:

the semiconductor substrate comprises a p-type silicon substrate;  
the source comprises an n+-type source region in the substrate;  
the drain comprises an n+-type drain region in the substrate;  
the channel comprises a channel region in the substrate between the source region and the drain region;  
the gate comprises a floating gate isolated from the channel region by the amorphous layer of carburized silicon; and

further comprising a polysilicon control gate separated from the floating gate by a layer of insulating material.

43.(New) The device of claim 3 wherein:

the semiconductor substrate comprises a p-type silicon substrate;  
the source comprises an n+-type source region in the substrate;  
the drain comprises an n+-type drain region in the substrate;  
the channel comprises a channel region in the substrate between the source region and the drain region; and

the control gate comprises a polysilicon control gate separated from the floating gate by a layer of insulating material.

44.(New) The transistor of claim 24 wherein:

the substrate comprises a p-type silicon substrate;  
the source region comprises an n+-type source region in the substrate; and  
the drain region comprises an n+-type drain region in the substrate.

45.(New) A transistor comprising:

an n+-type source region in a p-type silicon substrate;

an n+-type drain region in the substrate;  
a channel region in the substrate between the source region and the drain region; and  
a gate separated from the channel region by a layer of amorphous carburized silicon.

46.(New) A transistor comprising:  
a source region in a substrate;  
a drain region in the substrate;  
a channel region between the source region and the drain region in the substrate; and  
a floating gate separated from the channel region by a layer of amorphous carburized silicon.

47.(New) The transistor of claim 46 wherein:  
the substrate comprises a p-type silicon substrate;  
the source region comprises an n+-type source region in the substrate;  
the drain region comprises an n+-type drain region in the substrate; and  
further comprising a polysilicon control gate separated from the floating gate by a layer of insulating material.

48.(New) A transistor comprising:  
an n+-type source region in a p-type silicon substrate;  
an n+-type drain region in the substrate;  
a channel region between the source region and the drain region in the substrate;  
a floating gate separated from the channel region by a layer of amorphous carburized silicon; and  
a polysilicon control gate separated from the floating gate by a layer of insulating material.

49.(New) The memory cell of claim 21 wherein:  
the substrate comprises a p-type silicon substrate;  
the source region comprises an n+-type source region in the substrate;  
the drain region comprises an n+-type drain region in the substrate; and  
the control gate comprises a polysilicon control gate separated from the floating gate by a layer of insulating material.

50.(New) A memory cell comprising:

- a source region in a substrate;
- a drain region in the substrate;
- a channel region in the substrate between the source region and the drain region;
- a floating gate;
- a layer of amorphous carburized silicon between the floating gate and the channel region in the substrate; and
- a control gate separated from the floating gate.

51.(New) The memory cell of claim 50 wherein:

- 02.
- the substrate comprises a p-type silicon substrate;
  - the source region comprises an n+-type source region in the substrate;
  - the drain region comprises an n+-type drain region in the substrate; and
  - the control gate comprises a polysilicon control gate separated from the floating gate by a layer of insulating material.

52.(New) A memory cell comprising:

- an n+-type source region in a p-type silicon substrate;
- an n+-type drain region in the substrate;
- a channel region in the substrate between the source region and the drain region;
- a floating gate;
- a layer of amorphous carburized silicon between the floating gate and the channel region in the substrate; and
- a polysilicon control gate separated from the floating gate by a layer of insulating material.

53.(New) A semiconductor device comprising:

- a conductive layer supported by a substrate;
- a layer of amorphous carburized silicon in contact with the conductive layer; and
- a polysilicon layer in contact with the layer of amorphous carburized silicon.

54.(New) The semiconductor device of claim 53 wherein:

**AMENDMENT AND RESPONSE**

Serial Number: 08/903,453

Filing Date: July 29, 1997

Title: CARBURIZED SILICON GATE INSULATORS FOR INTEGRATED CIRCUITS

Page 5

Dkt: 303.378US1

the conductive layer comprises polysilicon; and  
the semiconductor device further comprises a source/drain diffusion in the substrate.

55.(New) A semiconductor device comprising:  
a first polysilicon layer supported by a substrate;  
a layer of amorphous carburized silicon in contact with the first polysilicon layer; and  
a second polysilicon layer in contact with the layer of amorphous carburized silicon.

56.(New) The semiconductor device of claim 55, further comprising a source/drain diffusion in the substrate.

57.(New) A memory cell comprising:  
a conductive layer supported by a substrate;  
a layer of amorphous carburized silicon in contact with the conductive layer; and  
a polysilicon layer in contact with the layer of amorphous carburized silicon.

58.(New) The memory cell of claim 57 wherein:  
the conductive layer comprises polysilicon; and  
the memory cell further comprises a source/drain diffusion in the substrate.

59.(New) A memory cell comprising:  
a first polysilicon layer supported by a substrate;  
a layer of amorphous carburized silicon in contact with the first polysilicon layer; and  
a second polysilicon layer in contact with the layer of amorphous carburized silicon.

60.(New) The memory cell of claim 59, further comprising a source/drain diffusion in the substrate.

61.(New) A capacitor comprising:  
a conductive layer supported by a substrate;  
a layer of amorphous carburized silicon in contact with the conductive layer; and  
a polysilicon layer in contact with the layer of amorphous carburized silicon.